Performance Characterization of Dual-Metal Triple- Gate-Dielectric (DM_TGD) Tunnel Field Effect Transistor (TFET)

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Abstract: Since, Dual Metal Gate (DMG) technology alone is not enough to rectify the problem of low ON current and large ambipolar current in the TFET, therefore, a novel TFET structure, known as dual metal triple-gate-dielectric (DM_TGD) TFET, has been proposed. We have combined the dielectric and gate material work function engineering to enhance the performance of the conventional FET. In the proposed structure, the gate region is divided into three dielectric materials: $TiO_2/Al_2O_3/SiO_2$. This approach is chosen because high dielectric material alone near the source cannot improve the performance due to increase in fringing fields. This paper presents the detail processing of the proposed structure. We have evaluated and optimized the dc performance of the proposed N-DM_TGD TFET with the help of 2-D ATLAS simulator. The results were compared with those exhibited by dual metal hetero-gate-dielectric TFET, single metal hetero- gate-dielectric TFET and single metal triple-gate-dielectric TFET of identical dimensions. It has been observed that the DM_TGD device offers better transconductance (gm), lower subthreshold slope, lower ambipolar current and larger ON current.

Keywords: Dual metal gate, Dielectric material, TFET, Subthreshold swing, DIBL, Ambipolar current, ON current.

1. INTRODUCTION

Earlier, miniaturization of MOSFET was the effective way to improve the performance of the circuit but in post scaling era the miniaturization of device is not becoming effective due to increased leakage current and short channel effects (SCEs) [1-3]. To overcome these limitations, researchers have proposed many different structures rather than planar in the literature [4-6] particularly multi gates devices and devices fabricated using different materials to replace the standard CMOS technology [7-9]. In nanoscale era, leakage current is major problem in the device which modifies the stable performance of the devices; therefore, suppression of leakage current without compromising the ON current is the major challenge. To control the leakage current, nanowire transistors have been proposed [10-12]. Among these, tunnel field-effect- transistors (TFETs) are considered one of the future devices to replace the planar MOSFETs [13-14]. Although TFET, possess lower subthreshold slope *(SS)* (< 60 mV/decade) at room temperature, but still, suffers from two main drawbacks; lower ON current and larger ambipolar current [15-16]. The ON current of TFET device can be increased by using high k- dielectric material as a gate insulator [17] on the cost of increased Iamb whereas TFET with gate-drain overlap structure have been proposed to reduce ambipolar current [18] on the cost of reduced chip density. In literature, hetero- dielectric gate (HDG) TFET is proposed to overcome these two shortcomings after using a high-*k* material partially near source to enhance the ON current and SiO_2 near drain to suppress the ambipolar current [19]. Although. HfO_2 has a reasonably high dielectric constant (~25) and a relatively large band gap (5.68 eV) but it is very difficult to convert pure HfO2 from amorphous to polycrystalline structure during the post- annealing treatment and also having poor interface quality with Si [20] which can be improved by incorporation of nitrogen in HfO_2 on the cost of lower dielectric constant [22]. Due to these reasons, the application of other metal oxides, with a dielectric constant higher than 25, in TFET device is very important. Titanium dioxide (TiO_2) appears as one of the alternative gate dielectric material to replace HfO_2 even though it has relatively small band gap (3.5 eV) [22]. Since, it is difficult to find a single oxide which satisfies high dielectric constant, low interface trap density, high thermal stability, for future gate dielectric, hence bilayer gate dielectrics is an alternative option. Researchers have used titania and alumina as reinforcements to improve the dielectric constant [23].

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In the proposed structure, we have chosen TiO_2/Al_2O_3 dielectric materials near the source and SiO_2 near drain [24]. According to researchers [25-26], dual metal gate (DMG) structures, having different work function metals (tunneling gate near source and auxiliary gate near drain), are effective way to reduce SCEs in the TFET device without any adverse effect. By considering the advantages associated with heterogeneous dielectric and DMG, this paper presents the combination of both engineering aspects to improve the performance of the TFET. The structure of this paper is given as follows: Section II describes the device structure, and the process flow steps. Section III describes the simulation results and discussion whereas section IV concludes the paper.

2. DEVICE STRUCTURE AND PROCESS FLOW

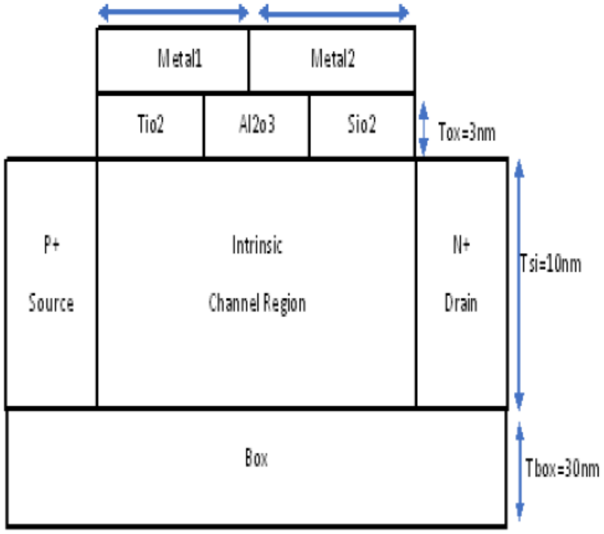

Figure 1(a): Structure of DM_TGD TFET [24].

The processing of the proposed structure (Figure **1**(**a**)) has been done using 2-D Silvaco ATHENA and ATLAS. The process steps follow the standard CMOS process in which P- type (100) SOI structure (*tsoi*=10 nm, *tbox*=3 nm) has been chosen to restrict the leakage current. On the top of intrinsic silicon oxide layer has been grown. The asymmetric source and drain doping profiles are obtained by ion implantation of boron dose of 1.0e20 cm-2 at 1 KeV (Figure **1**(**b**)(**i**)) and phosphorous dose of 1.0e18 cm-2 at 5 KeV (Figure **1**(**b**)) using nitride mask layer. This also results in steep junction profile as shown in Figure **1**(**b**)(**ii**). Since, the proposed structure's gate has been divided into three dielectric materials of thickness of 3 nm, we have first deposited TiO_2 near source (Figure **1**(**c**), second dielectric layer of Al_2O_3 is deposited using atomic layer deposition (ALD) (Figure **1**(**d**)) and finally third layer of

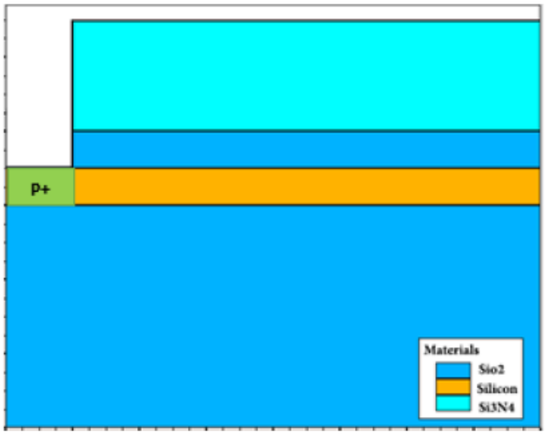

Figure 1(b)(i): Source region implantation.

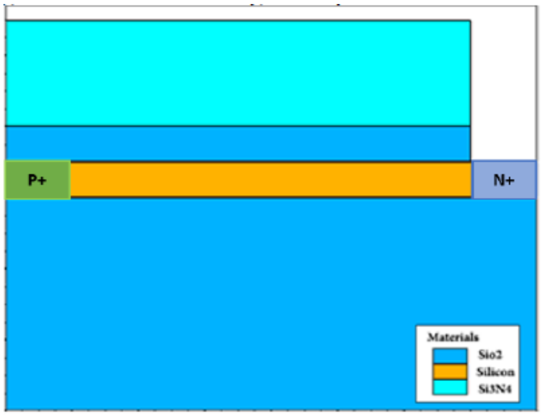

Figure 1(b)(ii): Drain region implantation.

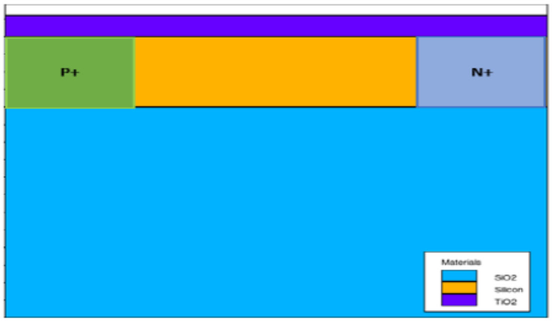

Figure 1(c)(i): TiO2 Dielectric deposition.

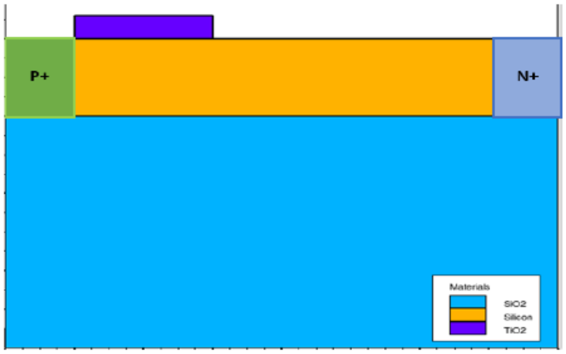

Figure 1(c)(ii): TiO2 Dielectric etching process.

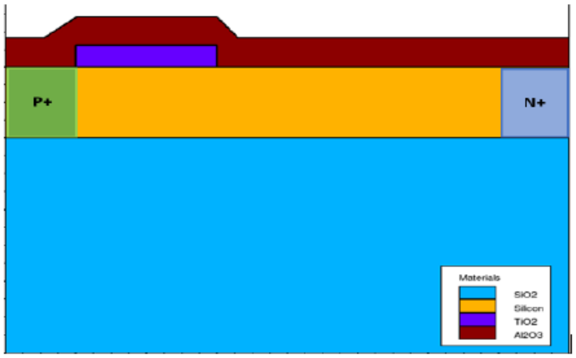

Figure 1(d)(i): Al2O3 Dielectric layer deposition process.

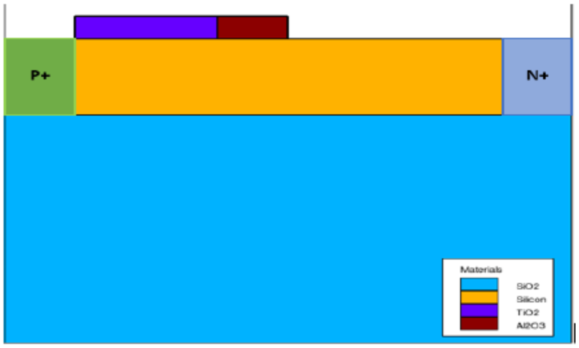

Figure 1(d)(ii): Al2O3 Dielectric layer Etching process.

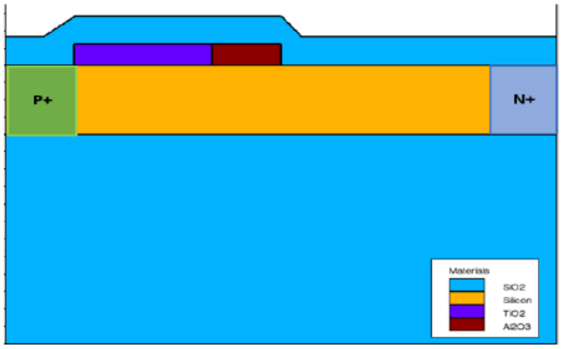

Figure 1(e)(i): SiO2 Dielectric layer deposition process.

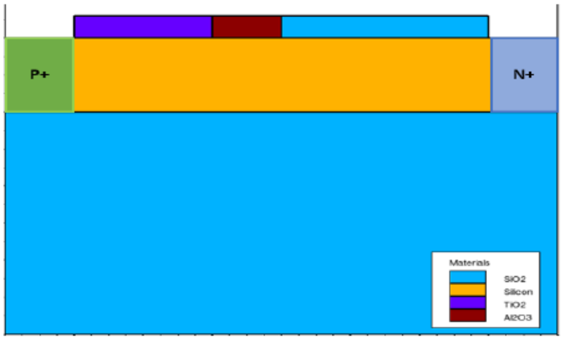

Figure 1(e)(ii): SiO2 Dielectric layer Etching process.

SiO_2, near drain, is deposited. After depositing each dielectric material on gate, we have performed selective etching to remove the unwanted layer (Figure **1**(**e**)). The first gate material is etched with a carefully controlled manner and then a second gate material is formed using conventional deposition process. The thickness of auxiliary gate and tunneling gate is 5-nm (Figure **1**(**f**)). Next, using PECVD process, we have formed sidewall spacer after deposition and etching of TEOS layer. We have used sputtering method to put Al-metal on the gate and at the source and drain contacts. Metal pads are defined by photolithography and etch process. The overall fabricated structure of the proposed device is shown in Figure **1**(**g**) [24].

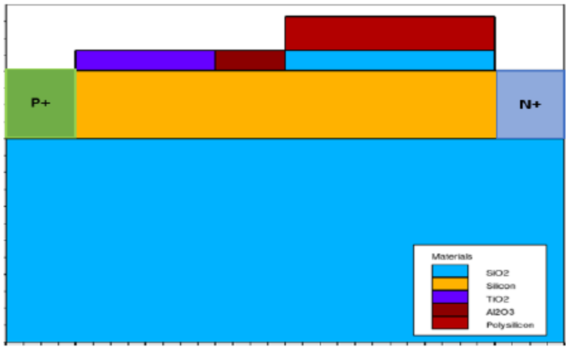

Figure 1(f)(i): Auxiliary gate formation.

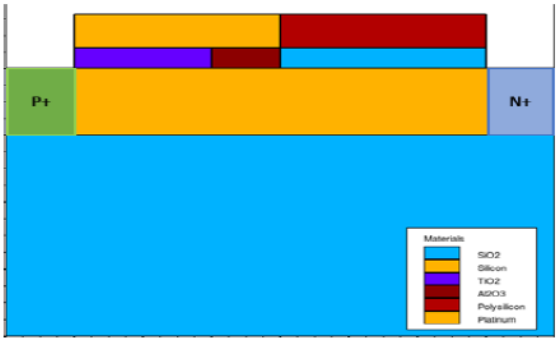

Figure 1(f)(ii): Tunneling gate formation.

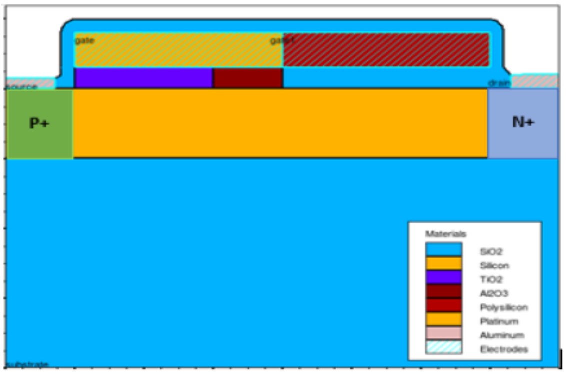

Figure 1(g): Final Structure of the proposed TFET [24].

3. SIMULATION RESULTS AND DISCUSSION

We have performed simulations of the proposed structure using 2-D Silvaco ATLAS tool. We have considered the non- local BTBT model, the band gap narrowing model, Fermi- Dirac statistics, Shockley-

Table 1: Comparison of SS, Iamb and ION for Three Different Combinations of Dielectric Materials

Type of Combination	Average SS (mV/Decade)	Iamb (pA/µm)	Ion (µA/µm)
ZrO_2-Al_2O_3-SiO_2	47.2	1.82	$7.6*10^{-2}$
HfO_2-Al_2O_3-SiO_2	47.3	1.82	$7.6*10^{-2}$
Proposed (TiO_2- Al_2O_3-SiO_2)	42.7	0.181	1.11
TiO_2-ZrO_2-SiO_2	42.8	1.82	1.04
TiO_2-HfO_2-SiO_2	42.8	1.82	1.04

Read-Hall (SRH) recombination and Lombardi mobility model during simulation. The values of various parameters during simulation were taken as; gate length Lg (L_{TiO2}+, L_{Al2O3}+L_{SiO2})= 60 nm, work function of two gate metals are 3.9 eV and 4.3 eV, tox= 3 nm, tsi=10 nm (hence quantum mechanical effect has been ignored in this study). ON-current (Ion) in this paper has measured as the drain current when V_{gs}=V_{ds}=1 V whereas ambipolar current (Iamb) is defined as the drain current when V_{gs}=-0.2 V and V_{ds}=1 V.

Table **1** gives the simulation results for various combinations of triple dielectric materials as an insulator for the proposed structure at V_{ds}=1 V and *Lhighκ*

(ZrO_2/HfO_2/TiO_2)= 20 nm, L_{Al2O3}=10 nm and L_{SiO2}=30 nm, L_{tunnel}=L_{aux}=30 nm. From simulation results, it is observed that TiO_2/Al_2O_3/SiO_2 combination as a gate insulator gives about 10% decrease in subthreshold swing SS, significant increase in ON-current and reduction in ambipolar current compared to other combination. These improvements are due to reduced EOT which results in better gate coupling at the source- channel interface and lower leakage current.

Due to the better performance in terms of ON current, ambipolar current and SS, we have chosen TiO_2/Al_2O_3/SiO_2 as a gate insulator for the further investigation of the electrical performance of DM_TGD TFET.

From simulation results, it has been observed that when L_{TiO2}=20 nm, L_{Al2O3}=10 nm and L_{SiO2}= 30 nm, larger ON current and lower ambipolar current results in proposed structure. This is due to fact that as L_{TiO2} decreases, the conduction band (CB) well becomes shallower which makes band-to-band tunneling difficult to occur. Therefore, L_{TiO2}=20 nm is the better choice for the performance improvement. After selecting the proper dielectric lengths, we simulated the TFET for optimizing the lengths of tunnel gate and auxiliary gate.

In TFETs, the electric field plays a very vital role in improving the ON current of the device. As the electric field increases at the tunnel junction, the tunneling probability of the electrons increases, thereby resulting in larger tunneling current. Figure **2**(**a**) shows that the peak electric field occurs near the tunneling junction irrespective of the choice of auxiliary and tunneling

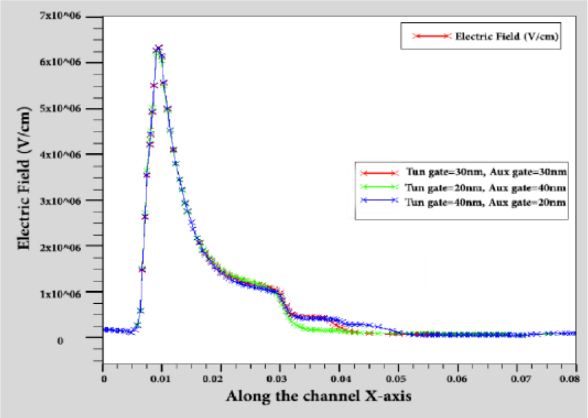

Figure 2 (a): Lateral electric field for different tunnel gate and auxiliary gate lengths.

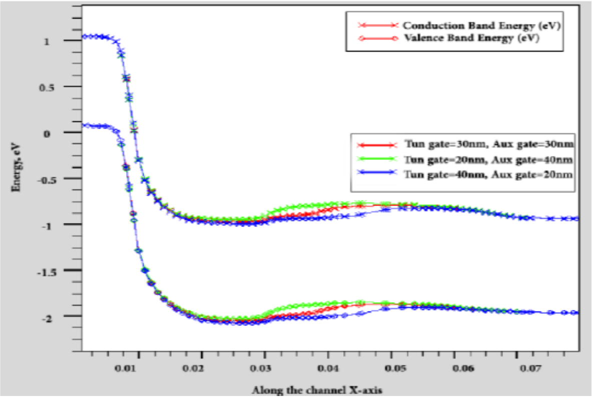

Figure 2(b): Band diagram for different combinations of tunnel length and auxiliary length.

lengths. It is also observed that when L_{tunnel}=40 nm *and* L_{aux}=*20* nm, electric filed takes lower value compared to the other combinations near the drain which suppress the ambipolar current in the device. The larger electric field near the source-channel junction narrows the tunneling width as shown in Figure **2**(**b**) which results in larger tunneling current (Figure **2**(**c**)).

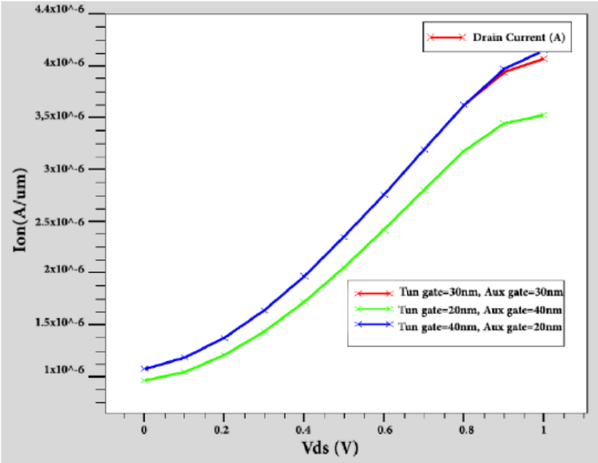

Figure 2(c): ON current for different combinations of tunnel and auxiliary lengths.

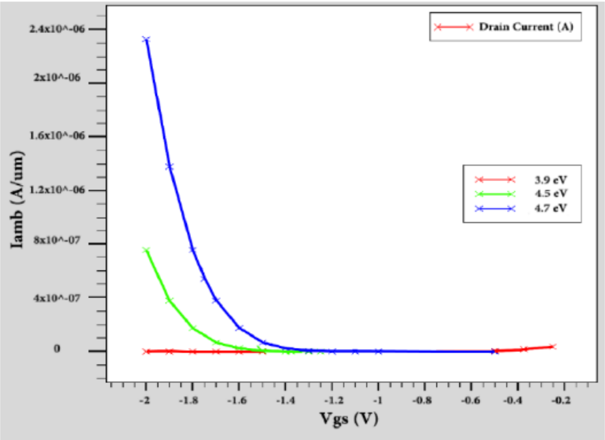

Figure 2(d): Ambipolar current variation with gate voltage for different tunnel-gate work function.

The variation of ambipolar current (Iamb) with *Vgs* for different tunnel-gate work function is shown in Figure **2**(**d**). The lower work function metal near source increases the band overlap which result in increased tunneling probability of electrons from valence band to conduction band of the channel.

Performance Comparison

After selecting the optimized values of the parameters, we have compared our proposed structure with dual metal hetero- gate-dielectric TFET and the results of various electrical performances are given in Table **2**. The proposed device gives higher ON current, lower subthreshold slope and ambipolar current compared to the dual metal hetero-gate dielectric TFET due to high effective dielectric constant, high interface quality and reduced insulating barrier near the source-channel junction which increases the probability of tunneling.

Table 2: Comparison with Hetero-gate Dielectric TFET

Different Combinations	*SS (mV/decade)*	*Iamb, (pA/μm)*	*Ion (mA/μm)*
Proposed (TiO_2-Al_2O_3-SiO_2)	42.7	0.181	11.01
DMGHD (TiO_2-SiO_2)	56	1.3	10.10
DMGHD (HfO_2-SiO_2)	47	0.6	7.60
DMGHD Stack	77	16	1.80

The electric filed in the proposed structure increases considerably compared to the single gate triple dielectric materials on the cost of slightly increased ambipolar current. Due to increased electric field in the proposed structure, the conduction as well as valence bands move upwards. This upward shift of the band reduces the tunneling width compare to other structure (Figure **3**(**a**)). Since, the generation rate exponentially increases with the electric field, hence an increase in electric field increases the generation rate which results in larger ON current (Figure **3**(**b**)) in the proposed TFET structure. This study only confirms that by combining the advantages of triple dielectric materials and dual metal gate in realizing the TFET structure, one can improve the performance of the device.

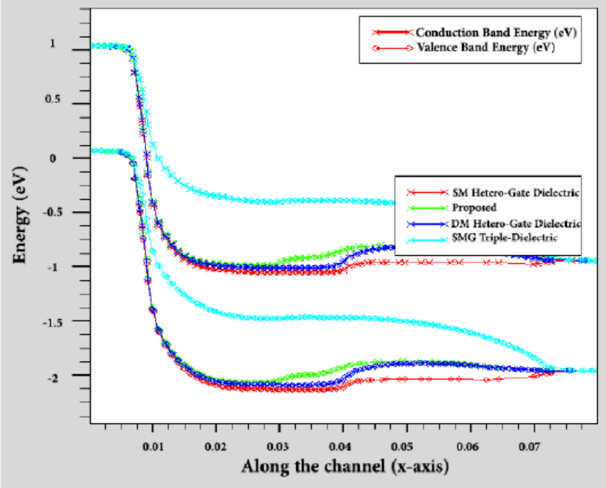

Figure 3(a): Band Diagram for various TFET structures.

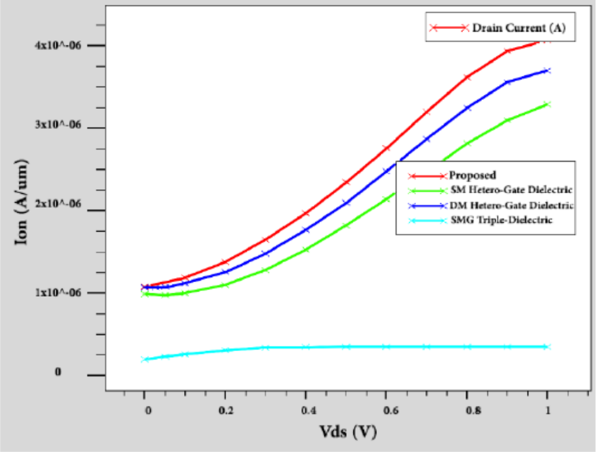

Figure 3(b): ION comparison for different structures.

Transconductance of the device plays a crucial role in determining the cut-off frequency. The variation in transconductance w.r.t. the gate voltage is shown in Figure **3**(**c**). The proposed TFET structure exhibits higher transconductance compared to the single metal/dual metal hetero-gate-dielectric TFET because of increase in tunnelling probability at the source-channel junction and controlled leakage current as well as lower trap density.

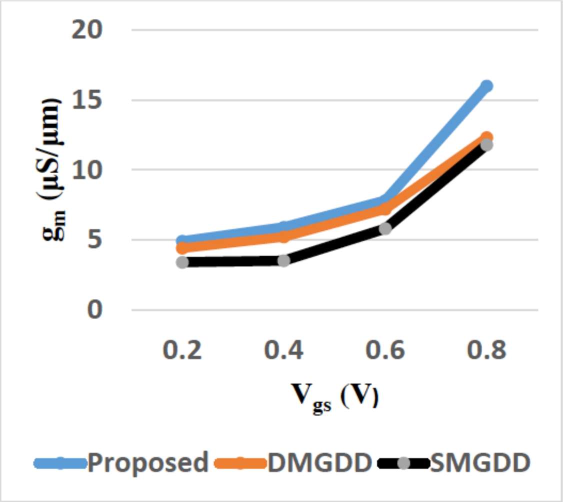

Figure 3(c): Variation of gm with Vgs for proposed and Hetero-dielectric TFETs.

4. CONCLUSION

A TFET device with dual metal triple-gate-dielectric tunnel configuration is presented for the suppression of ambipolar current with improved ON current and reduced short channel effects. The combination of dielectric and gate engineering approach not only increases the ON current compared to the dual metal hetero-gate-dielectric TFET but also reduces ambipolar current, enhances the transconductance and reduces the threshold voltage. The device is fabricated with 2-D Silvaco ATHENA tools based on the optimized parameters and simulated with ATLAS simulator. The choice of lateral combination of TiO2 and Al2O3 side by side as a gate insulator near source reduces the fringe field and enhances the coupling between gate and source which results in increase of the ON current. The dielectric combination near the source also reduces the insulating barrier, trap charge density at the source and produces the high interface quality with reduced leakage current. In future it is required to develop compact analytical models to characterize the proposed structure. These models should be incorporated into spice simulator for deep understanding of the proposed device.

REFERENCES

[1] D'Agostino F, Quercia D. "Short-channel effects in MOSFETs", Proc. Introduction VLSI Design (EECS 467), pp. 1-15, Dec. 2000.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, Oxford: Clarendon, 1892; 2(3): 68-73.

[2] Chaudhry A, Kumar MJ. "Controlling short-channel effects in deep submicron SOI MOSFET's for improved reliability: A review", IEEE Trans. Device Mater. Rel 2004; 4(1): 99-109. https://doi.org/10.1109/TDMR.2004.824359

[3] M. Ali Pourghaderi, Anh-Tuan Pham, Hesameddin Hatikhameseh, Jongchol Kim, Hong-Hyun Park, Seonghoon Jin, Won-Young Chung, Woosung Choi, Shigenobu Maeda, Keun-Ho Lee, "Universality of Short-Channel Effects on Ultrascaled MOSFET Performance", IEEE Electron Device Letters, 2018; 39(2): 168-171. https://doi.org/10.1109/LED.2017.2784099

[4] Riyadi MA, Suseno JE, Ismail R. "The future of no-planar nanoelectronics MOSFET devices: A revies", J. Applied Science, 2010; 10: 2136-2146. https://doi.org/10.3923/jas.2010.2136.2146

[5] D. Bhattacharya, NK. Jha, "FinFETs: From devices to architectures", Adv. Electron vol. 2014; pp. 1-21. https://doi.org/10.1155/2014/365689

[6] Ravi Shankar Pal, Savitesh Sharma, Sudeb Dasgupta, "Recent trend of FinFET devices and its challenges: A review", 2017 Conference on Emerging devices and Smart Systems (ICEDSS).

[7] JP. Colinge, FinFETs and other Multi-Gate Transistors, New York, NY, USA:Springer Science+ Bussiness Media, 2008. https://doi.org/10.1007/978-0-387-71752-4

[8] SL. Tripathi, R. Mishra, RA. Mishra, "Multi-gate MOSFET structures with high- k dielectric materials", J. Electron Devices 2012; 16: 1388-1394.

[9] Jansung Park, Sung-Min Hong, "Simulation study of enhancement mode Multi-Gate vertical Gallium Oxide MOSFETs", ECS journal of Solid State Science and Technology 2019; 8(7): Q3116-Q3121. https://doi.org/10.1149/2.0181907jss

[10] Lu W, Xie P, Lieber CM. "Nanowire transistor performance limits and applications", IEEE Trans. Electron Devices 2008; 55(11): 2859-2876. https://doi.org/10.1109/TED.2008.2005158

[11] Su PC, Chen BH, Lee YC, Yang YS. "Silicon Nanowire Field-Effect Transistor as Biosensing Platforms for Post-Translational Modification", Biosensors, 2020; 10: pp. 213. https://doi.org/10.3390/bios10120213

[12] Chang SM, Palanisamy S, Wu TH, *et al.* " Utilization of silicon nanowire field-effect transistors for the detection of a cardiac biomarker, cardiac troponin I and their applications involving animal models", Sci Rep 2020; 10: pp. 22027. https://doi.org/10.1038/s41598-020-78829-7

[13] Choi WY, Park BG, Lee JD, Liu TJK. "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec", IEEE Electron Device Lett 2007; 28(8): 743-745. https://doi.org/10.1109/LED.2007.901273

[14] Priya GL, Venkatesh M, Balamurugan NB. *et al*. Triple Metal Surrounding Gate Junctionless Tunnel FET Based 6T SRAM Design for Low Leakage Memory System. Silicon 2021; 13: 1691-1702. https://doi.org/10.1007/s12633-021-01075-7

[15] Avci UE, Morris DH, Young IA. "Tunnel field-effect transistors: Prospects and challenges", IEEE J. Electron Devices Soc 2015; 3(3): 88-95. https://doi.org/10.1109/JEDS.2015.2390591

[16] Reddy NN, Panda DK. A Comprehensive Review on Tunnel Field- Effect Transistor (TFET) Based Biosensors: Recent Advances and Future Prospects on Device Structure and Sensitivity. Silicon, 2020. https://doi.org/10.1007/s12633-020-00657-1

[17] HW. Kim *et al.*, "A tunneling field-effect transistor using side metal gate/high-k material for low power application," 2011 International Semiconductor Device Research Symposium (ISDRS), 2011; pp. 1-2.

[18] Anne Verhulst, Karen Maex, Guido Groeseneken, "Tunnel-Field Effect transistor without gate-drain overlap", Applied Physics Letters, 2007; 91(5). https://doi.org/10.1063/1.2757593

[19] Choi WY, Lee HK. "Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs)", Nano Converg 2016; 3(1): 1-15. https://doi.org/10.1186/s40580-016-0073-y

[20] M. Shunqukela and VM. Srivastava, "Dielectric Material (HfO2) Effect on Surface Potential for CSDG MOSFET," 2018 International Conference on Computer Communication and Informatics (ICCCI), 2018; pp. 1-5. https://doi.org/10.1109/ICCCI.2018.8441369

[21] Y. Zhang, W. Lin, Y. Li, K. Ding, and JQ. Li, "A theoretical study on the electronic structures of TiO2: effect of Hartree-Fock exchange," Journal of Physical Chemistry B 2005; 09(41): 19270-19277. https://doi.org/10.1021/jp0523625

[22] Bonkerud J, Zimmermann C, Weiser PM. *et al*. On the permittivity of titanium dioxide. Sci Rep 2021; 11: pp. 12443. https://doi.org/10.1038/s41598-021-92021-5

[23] Raborty KY. Raj, AK. Pradhan, B. Chatterjee, S. Chakravorti, S. Dalai, "Investigation of Dielectric Properties of TiO2 and Al2O3 nanofluids by Frequency Domain.

[24] Ajay Kumar Singh, and Tan Chun Fui, "Dual Metal Triple-gate- dielectric (DM_TGD) Tunnel Field Effect Transistor: A Novel Structure for Future Energy Efficient Device" Recent Advances in Electrical and Electronic Engineering (EENG), 2021; 6.

[25] Krauss T, Wessely F, Schwalke U. "Eletrically reconfigurable dual metal-gate planar field-effect transistor for dopant-free CMOS", 13th International Multi-Conference on Systems Signals & Devices, 2016. https://doi.org/10.1109/SSD.2016.7473724

[26] Paul A, Saha P and Malakar TD. "Study of Device Performance of Dual Metal Gate Silicon on Insulator MOSFET Adopting Various Dielectric Materials in Gate Oxide," 2020 IEEE VLSI Device Circuit and System (VLSI DCS), 2020; pp. 229-233. https://doi.org/10.1109/VLSIDCS47293.2020.9179873

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